AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A method for forming an electronic device having a multilayer structure, comprising:

embossing a surface of a substrate so as to depress first and second regions of the substrate relative to at least a third region of the substrate;

applying a solution of a ~~depositing~~ conductive or semiconductive material ~~from solution~~ onto the substrate so as to confine in a single step the deposition of said conductive or semiconductive material to said first and second regions, whereby the conductive or semiconductive material forms a first electrode on the first region and a second electrode on the second region, wherein the first and second electrodes are electrically insulated from each other by the third region.

2. (currently amended): A method as claimed in claim 1, wherein ~~the width of~~ the third region has a width ~~is~~ defined by ~~the~~ a depth to which ~~of~~ embossing is performed.

3. (currently amended): A method as claimed in claim 2, wherein the step of embossing is performed with a tool having an embossing surface, the embossing surface of the tool bearing at least one protruding portion having a sharp protruding tip wherein ~~the width of~~ the protruding portion has a width that widens from the sharp protruding tip, towards the embossing surface of the tool such that the width of a depressed region of the substrate, as measured in ~~the~~ a plane of the surface of the substrate, is dependent on ~~the~~ a depth ~~of incursion of~~to which the at least one protruding ~~edge~~ portion of the tool enters into the substrate.

4. (currently amended): A method as claimed in claim 2, wherein the step of embossing is performed with a tool having an embossing surface, the embossing surface of the tool bearing at least one recessed portion having a recessed point wherein ~~the width of~~ the recessed portion has a width that widens from the recessed point, towards the embossing surface of the tool such that ~~the width of~~ a raised region of the substrate has a width, as measured in ~~the~~ a

plane of the surface of the substrate, is dependent on ~~the~~ a depth ~~of incursion of~~to which the embossing surface of the tool enters into the substrate.

5. (currently amended): A method as claimed in claim 1, wherein after the step of embossing and prior to the step of depositing a solution of conductive or semiconductive material, the method further comprises the step of:

treating the surface of the substrate with a surface modification process that has a different effect on ~~the~~ depressed regions of the substrate relative to ~~the~~ non-depressed regions of the substrate whereby the ~~raised~~ non-depressed regions and the depressed regions are given different surface energies, such that the deposition of the material is defined by the surface energy of the substrate in the first and second regions.

6. (currently amended): A method as claimed in claim 1, wherein the third region is a ridge wherein ~~the width of~~ the ridge has a width that defines a length of a channel of the electronic device.

7. (original): A method as claimed in claim 6, wherein a cross section of the ridge is substantially rectangular.

8. (original): A method as claimed in claim 6, wherein a cross section of the ridge is substantially triangular.

9. (currently amended): A method as claimed in claim 1, wherein the embossing step is performed at a temperature within 50 °C of the glass transition temperature of ~~the~~ a topmost surface of the substrate.

10. (currently amended): A method as claimed in claim 1, wherein the embossing step is performed at a temperature at which ~~the~~ a topmost surface of the substrate is in a liquid phase.

11. (currently amended): A method as claimed in claim 1, wherein the substrate comprises a flexible plastic substrate such as poly(ethyleneterephthalate)~~ethleneterephtalate)~~ (PET), polyethersulphone (PES) or ~~polyethernaphtalene~~ polyethernaphthalene(PEN).

12. (previously presented): A method as claimed in claim 1, wherein the substrate comprises a rigid substrate coated with a polymer layer.

13. (currently amended): A method as claimed in claim ~~4~~ 5, wherein said treating step comprises using a polymer layer ~~with~~ having a high surface energy as the substrate.

14. (currently amended): A method as claimed in claim ~~4~~ 5, wherein said treating step comprises exposing the substrate to one or more of an oxygen plasma, carbon-tetrafluoride plasma, ultra-violet or ozone surface treatment.

15. (currently amended): A method as claimed in claim ~~8~~ 5, wherein said treating step comprises depositing a surface modifying layer onto the substrate at an oblique angle such that the surface modifying material is deposited onto the ~~raised~~ non-depressed portions of the substrate, and the depressed portions are shadowed by the ~~raised~~ non-depressed portions during the deposition of the surface modifying layer.

16. (currently amended): A method as claimed in claim ~~4~~ 5, wherein said treating step comprises exposing the substrate to a physical etching method such as reactive ion etching.

17. (currently amended): A method as claimed in claim ~~4~~ 5, wherein said treating step comprises applying a flat stamp to the surface.

18. (original): A method as claimed in claim 17, wherein the flat stamp is inked with a self-assembled monolayer.

19. (original): A method as claimed in claim 18, wherein the self-assembled monolayer is capable of bonding with functional groups on the surface of the substrate.

20. (previously presented): A method as claimed in claim 18, wherein the self-assembled monolayer is octyltrichlorosilane or fluoroalkyltrichlorosilane.

21. (original): A method as claimed in claim 18, wherein the self-assembled monolayer comprises a methoxy silane.

22. (previously presented): A method as claimed in claim 1, wherein the solution of conductive or semiconductive material comprises a conductive ink.

23. (original): A method as claimed in claim 22, wherein the conductive ink comprises a conductive polymer.

24. (original): A method as claimed in claim 23, wherein the conductive polymer is polyethylenedioxythiophene doped with polystyrene sulfonic acid (PEDOT/PSS).

25. (original): A method as claimed in claim 22, wherein the conductive ink comprises a conductive inorganic dispersion of electrically conductive nanoparticles.

26. (currently amended): A method as claimed in claim 22, wherein the conductive ink comprises a solution of ~~chemical precursor solution for~~ an inorganic metal precursor ~~formulated in a solvent~~.

27. (currently amended): A method as claimed in claim 1, further comprising the step of depositing a layer of semiconductive material over the substrate and ~~conductive or semiconductive material~~ first and second electrodes.

28. (currently amended): A method as claimed in claim 27, wherein ~~said~~ the semiconductive material formed over the substrate and first and second electrodes is regioregular poly(3-hexylthiophene) (P3HT) or poly(dioctylfluorene-co-bithiophene) (F8T2).

29. (currently amended): A method as claimed in claim 27, wherein the ~~said~~ semiconductive material formed over the substrate and first and second electrodes is an inorganic nanoparticulate or an inorganic nanowire semiconductor.

30. (previously presented): A method as claimed in claim 27, further comprising the step of depositing a layer of dielectric over the layer of semiconductive material.

31. (original): A method as claimed in claim 30, wherein the layer of dielectric comprises a polymer layer.

32. (currently amended): A method as claimed in claim 31, wherein the polymer layer is ~~poly(methylmethracrylate)~~ poly(methylmethacrylate) (PMMA).

33. (previously presented): A method as claimed in claim 29, further comprising the step of printing a pattern of conductive material to form an electrode for said electronic device.

34. (original): A method as claimed in claim 33, wherein the electrode is formed from a conductive polymer or an inorganic material.

35. (previously presented): A method as claimed in claim 29, wherein both the semiconductor layer and the dielectric layer are patterned so as to form an active layer island of the device.

36. (previously presented): A method as claimed in claim 1, wherein the electronic device is a transistor.

37. (previously presented): A method as claimed in claim 1, wherein conductive material is deposited on the substrate which forms source and drain electrodes of the electronic device.

38. (previously presented): A method as claimed in claim 30, wherein the layer of dielectric deposited over the semiconductive layer is a gate dielectric layer.

39. (original): A method as claimed in claim 38, further comprising the step of depositing a gate electrode onto the surface of the gate dielectric layer.

40. (previously presented): A method as claimed in claim 1, wherein the embossing step is performed with a tool having an embossing surface suitable for embossing the substrate, the embossing surface bearing an array of protruding features with sharp tips.

41. (currently amended): A method as claimed in claim 40, wherein the sharp tips have a radius of curvature of ~~the sharp edges is~~ less than 100 μm.

42. (currently amended): A method as claimed in claim 40, wherein the sharp tips have a radius of curvature of ~~the sharp edges is~~ less than 10 μm.

43. (original): A method as claimed in claim 40, wherein the protruding features have a rectangular profile.

44. (currently amended): A method as claimed in claim 1, wherein ~~the width of~~ the third region has a width of ~~is~~ less than 20 μm.

45. (currently amended): A method as claimed in claim 1, wherein ~~the width of~~ the third region has a width of ~~is~~ less than 5 μm.

46. (currently amended): A method as claimed in claim 1, wherein ~~the width of~~ the third region has a width of ~~is~~ less than 1 μm.

47. (previously presented): A method as claimed in claim 1, wherein the substrate comprises a functional layer of the electronic device, wherein the functional layer comprises one of a conducting material and a semiconducting material.

48. - 122. (canceled)

123. (new): A method as claimed in claim 1, wherein the first and second electrodes are source and drain electrodes of a transistor.